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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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KEUSEY, TUTUNJIAN & BITETTO, P.C.			ROSSOSHEK, YELENA	
20 CROSSWAYS PARK NORTH			ART UNIT	PAPER NUMBER
SUITE 210			2825	
WOODBURY, NY 11797				

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

(3)

Office Action Summary	Application No.	Applicant(s)	
	10/687,475	FILIPPI ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 27 February 2006.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-32 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

<p>1)<input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</p> <p>2)<input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</p> <p>3)<input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.</p>	<p>4)<input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.</p> <p>5)<input type="checkbox"/> Notice of Informal Patent Application (PTO-152)</p> <p>6)<input type="checkbox"/> Other: _____.</p>
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DETAILED ACTION

1. This office action is in response to the Application 10/687,475 filed 10/16/2003 and amendment filed 02/27/2006.

2. Claims 1-32 remain pending in the Application. Claim 32 has been added to the Application.

3. Applicant's arguments have been fully considered and are persuasive. However, upon further consideration, a new ground(s) of rejection is made in view of Corson et al. (US Patent 6,629,292).

Claim Objections

4. Claims 11, 21, 30 are objected to because of the following informalities:

claim 11 line 2 after "instructions" delete "executable" insert --, which when executed--

claim 11 line 2 after "machine" delete "to perform" insert --performs--

The same changes have to be applied to claims 21 and 30.

Also has to be noted, that it is unclear what is useful concrete or tangible result produced by the claim as required under 35 USC § 101. Examiner recommends that Applicant must insert for clarification and definiteness the steps to be performed in claim 1 as required in claim 11. Claim 1 during the course of prosecution may be cancelled or is a subject to change. The same changes have to be applied to claims 21 and 30 according their relationships with claims 13 and 23 respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-11, 13-21 and 23-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lorenz et al. (US Application Publication 2005/0066301).

With respect to claim 1 Lorenz et al. teaches a method for analyzing circuit designs by using 3D numerical analysis of the governing partial differential equations (PDE) (paragraph [0001]), wherein PDE analyses a discrete element model of the integrated circuit design (paragraph [0009]), comprising the steps of: discretizing a design representation into pixel elements representative of a structure in the design where each pixel element represents a portion of the design within generating a discrete element model 170 as shown on the Fig. 1A, wherein discrete element model 170 includes a mesh 171 created by mesh generator tool 145 out of integrated circuit design information including a schematic 130 (paragraph [0023]) and mesh represents components of the integrated circuit design (paragraph [0028]) and wherein the mesh representation is normally created by subdividing the geometric shapes that comprise the device into smaller simpler shapes called finite elements (pixel elements), wherein mesh generator includes computer instructions describing how to create a mesh for

each component (finite element/pixel element) of the integrated circuit (MEMS) design (paragraphs [0006], [0027], [0010]); determining at least one property for each pixel element representing the portion of the design where the at least one property is represented by an intensity of the pixel element within creating the mesh representation of the corresponding components, wherein each component is characterized by parameter information, design information as fabrication process description and **material properties** (paragraph [0027]), wherein **mesh density (intensity) of each individual mesh** is a subject of analysis and adjusting as a step of integrated circuit (MEMS) design (claim 5 of Lorenz); and determining a response of the design due to local properties across the design based upon representations of the pixel elements, wherein within step 426 as shown on the Fig. 6, wherein the discrete element model including generated overall mesh created from individual meshes (step 424) is fed into a numerical solver to verify the assumptions made in creating the schematic of the integrated circuit or portion of it (paragraph [0034]), wherein generating the mesh representing a schematic MEMS design includes generating a plurality of individual meshes for the **plurality of components (pixel elements)** of the schematic MEMS design (claim 4 of Lorenz), wherein the analysis of the MEMS design programmatically analyzes **mesh density (intensity)** of each individual mesh of corresponding component (pixel element/finite element) (claim 5 of Lorenz).

With respect to claim 13 Lorenz et al. teaches a method for analyzing circuit designs by using 3D numerical analysis of the governing partial differential equations (PDE) (paragraph [0001]), wherein PDE analyses a discrete element model of the

integrated circuit design (paragraph [0009]), comprising the steps of: discretizing a design representation into pixel elements representative of a structure in the design where each pixel element represents a portion if the design within generating a discrete element model 170 as shown on the Fig. 1A, wherein discrete element model 170 includes a mesh 171 created by mesh generator tool 145 out of integrated circuit design information including a schematic 130 (paragraph [0023]) and mesh represents components of the integrated circuit design (paragraph [0028]) and wherein the mesh representation is normally created by subdividing the geometric shapes that comprise the device into smaller simpler shapes called finite elements (paragraph [0006]), wherein mesh generator includes computer instructions describing how to create a **mesh for each component (finite element/pixel element)** of the integrated circuit (MEMS) design (paragraphs [0006], [0027], [0010]); analyzing properties in each pixel element to represent the properties by an intensity of the pixel element within creating the mesh representation of the corresponding components, wherein each component is characterized by parameter information, design information as fabrication process description and **material properties** (paragraph [0027]), which are analyzed in the PDE solver for the analysis of the integrated circuit design (paragraph [0010]), wherein **mesh density (intensity) of each individual mesh** is a subject of analysis and adjusting as a step of integrated circuit (MEMS) design (claim 5 of Lorenz); assembling pixel properties to determine properties of a local three-dimensional circuit architecture within step 426 as shown on the Fig. 6, wherein the discrete element model including generated overall mesh created from individual meshes (step 424), wherein mesh is

generated from 3D solid model derived from the schematic as shown on the Fig. 3 (paragraphs [0017], [0021]); and determining a global response of the circuit architecture due to local properties across the design based upon representations of the pixel elements by feeding the discrete-element model into a numerical solver to verify the assumptions made in creating the schematic of the integrated circuit or portion of it as shown in step 426 of the Fig. 6 (paragraph [0034]), wherein generating the mesh representing a schematic MEMS design includes generating a plurality of individual meshes for the **plurality of components (pixel elements)** of the schematic MEMS design (claim 4 of Lorenz), wherein the analysis of the MEMS design programmatically analyzes **mesh density (intensity)** of each individual meshes of corresponding component (pixel element/finite element) (claim 5 of Lorenz).

With respect to claim 23 Lorenz et al. teaches a method for analyzing circuit designs by using 3D numerical analysis of the governing partial differential equations (PDE) (paragraph [0001]), wherein PDE analyses a discrete element model of the integrated circuit design (paragraph [0009]), comprising the steps of: importing a digitally rendered representation of a design within the system-level design and design environment 110 shown on the Fig. 1A, which allows a user to digitally compose integrated circuit schematic using a graphical interface (paragraph [0022]); discretizing the design representation into pixel elements representative of a structure in the design where each pixel element represents a portion of the design within generating a discrete element model 170 as shown on the Fig. 1A, wherein discrete element model 170 includes a mesh 171 created by mesh generator tool 145 out of integrated circuit design

information including a schematic 130 (paragraph [0023]) and mesh represents components of the integrated circuit design (paragraph [0028]) and wherein the mesh representation is normally created by subdividing the geometric shapes that comprise the device into smaller simpler shapes called finite elements (paragraph [0006]) wherein mesh generator includes computer instructions describing how to create a **mesh for each component (finite element/pixel element)** of the integrated circuit (MEMS) design (paragraphs [0006], [0027], [0010]); analyzing properties in each pixel element by calculating the properties based on geometrical features in the design where the properties are represented by an intensity of the pixel element within creating the mesh representation of the corresponding components, wherein each component is characterized by parameter information including a **component's position, orientation, length, width, height**, design information as fabrication process description and material properties (paragraph [0027]), which are analyzed in the PDE solver for the analysis of the integrated circuit design (paragraph [0010]) wherein **mesh density (intensity) of each individual mesh** is a subject of analysis and adjusting as a step of integrated circuit (MEMS) design (claim 5 of Lorenz); assembling pixel properties in geometrical regions to determine properties of a local three-dimensional circuit architecture within step 426 as shown on the Fig. 6, wherein the discrete element model including generated overall mesh created from individual meshes (step 424), wherein mesh is generated from 3D solid model derived from the schematic as shown on the Fig. 3 (paragraphs [0017], [0021]); and determining a global response of the circuit architecture due to the local properties across the design based upon

representations of the pixel elements by feeding the discrete-element model into a numerical solver to verify the assumptions made in creating the schematic of the integrated circuit or portion of it as shown in step 426 of the Fig. 6 (paragraph [0034]), wherein generating the mesh representing a schematic MEMS design includes generating a plurality of individual meshes for the **plurality of components (pixel elements)** of the schematic MEMS design (claim 4 of Lorenz), wherein the analysis of the MEMS design programmatically analyzes **mesh density (intensity)** of each individual meshes of corresponding component (pixel element/finite element) (claim 5 of Lorenz).

With respect to claims 11, 21 and 30 Lorenz et al. teaches a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for analyzing circuit designs within conventional CAD system, wherein the mesh generators are computer instructions describing how to create a mesh for the associated component of the integrate circuit design (paragraph [0010]).

With respect to claims 2-10, 14-20, 24-29 Lorenz et al. teaches:

Claims 2, 14, 24: further comprising the step of exporting pixel properties to an application within the behavioral model and mesh generator associated with each component has share the same parameters and wherein the generator itself is a procedure that uses the parameter information (properties) (paragraph [0027]);

Claim 3: further comprising the step of assembling pixel properties to determine local three-dimensional properties within step 426 as shown on the Fig. 6, wherein the

discrete element model including generated overall mesh created from individual meshes (step 424), wherein mesh is generated from 3D solid model derived from the schematic as shown on the Fig. 3 (paragraphs [0017], [0021]) and within creating the mesh representation of the corresponding components, wherein each component is characterized by parameter information including a component's position, orientation, length, width, height, design information as fabrication process description and material properties (paragraph [0027]);

Claim 4: wherein the step of determining a response of the design due to local properties across the design includes the step of determining a global response for an architecture due to the local three-dimensional properties by feeding the discrete-element model into a numerical solver to verify the assumptions made in creating the schematic of the integrated circuit or portion of it as shown in step 426 of the Fig. 6 (paragraph [0034]), wherein creating the mesh representation of the corresponding components includes characterizing each component by parameter information including a component's position, orientation, length, width, height, design information as fabrication process description and material properties (paragraph [0027]);

Claims 5, 15: further comprising the step of importing a design to be analyzed within the system-level design and design environment 110 shown on the Fig. 1A, which allows a user to digitally compose integrated circuit schematic using a graphical interface (paragraph [0022]);

Claims 6, 16, 25 : wherein the design includes a computer generated design of one of a circuit and a chip within conventional CAD system, wherein the mesh

generators are computer instructions describing how to create a mesh for the associated component of the integrate circuit design (paragraphs [0010]; [0004]);

Claims 7, 17, 26: wherein the at least one property includes metal fraction and the global response includes thermal strain within creating the mesh representation of the corresponding components, wherein each component is characterized by parameter information, design information as fabrication process description and **material properties** (paragraph [0027]) and PDE solver is used to obtain 3D simulation results for at least on of mechanical, electrostatic, magnetic, thermal, **electrothermal**, piezoelectric, piezo-resistive, fluid damping and electromagnetic effects;

Claims 8, 18, 27: the step of determining a response of the design includes accepting or rejecting a design based on the response as shown in the example demonstrated by Fig. 5 depicting the result of analyzing the design, wherein mesh represents interconnections of a few beam components, which needs to be modified (rejecting a design based on the response) (paragraphs [0031]; [0033])

Claims 9, 19, 28: further comprising the step of altering a design based on the response within customizing the mesh generators by user in order to address specific geometrical requirements (paragraphs [0031], [0033]);

Claims 10, 20, 29: wherein the step of determining a response further includes representing a three-dimensional multi-layered design in two dimensions such that properties within all layers are accumulated and represented in the two-dimensional image as shown on the Fig. 4, wherein the comb components 212 in the schematic 200

are selected and autogenerated mesh 300 is created as two-dimensional image (paragraphs [0027], [0028]).

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claim 32 is rejected under 35 U.S.C. 102(e) as being anticipated by Corson et al. (US Patent 6,629,292).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claim 32 Corson et al. teaches a method for analyzing circuit designs (col. 1, II.6-11; col. 20, II.59-61), comprising the steps of: discretizing a design representation into pixel elements representative of a structure in the design within a method for forming gray scale images in a semiconductor process (col. 4, II.45-48) using pixel design schemes during semiconductor manufacturing process (col. 4, II.63-65) and as shown on the Fig. 1b contiguous group of four pixel, each being of a different

gray level (discretizing) (col. 5, ll.4-6); determining at least one property for each pixel element representing a portion of the design wherein the at least one property includes metal fraction information relating to a metal fraction of structures in the portion as shown in the Fig. 4b, which represents a portion of the semiconductor substrate and presenting pixel element, which is the same as depicted on the Fig. 4a, (col. 5, ll.47-50), wherein one of the required characteristics (property) is density (col. 5, ll.60-62; 38-46); and determining a response of the design die to local properties across the design within analyzing a density reflects the level of metallization by having different level darkness (density) of a metal layer (col. 5, ll.65-67; col. 6, ll.1-8).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 12, 22, 31 are rejected under 35 U.S.C. 103(a) as being obvious over Lorenz et al. in view of Corson et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject

matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(I)(1) and § 706.02(I)(2).

With respect to claims 12, 22, 31 Lorenz teaches the limitations from which the claims depend. However, even Lorenz discloses analysis of the individual mesh's density which varies with light reflection from different materials having different thickness, lacks specifics regarding metal fraction information. Corson et al. teaches the at least one property includes metal fraction information relating to the metal fraction of stacked via structures within analyzing a density reflects the level of metallization by having different level darkness (density) of a metal layer (col. 5, ll.65-67; col. 6, ll.1-8), wherein multilayered semiconductor is depicted having different level of density (metal fraction) (col. 9, ll.32-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Corson et al. to teach the specifics subject matter Lorenz et al. does not teach, because the method for converting any image into a two dimensional pattern of contrasting materials which in turn is capable of rendering a visually perceptible image with a high degree of resolution and details (col. 1, ll.51-54).

Remarks

7. In the remarks applicant argues in substance:

- a) Lorenz does not define properties of a portion of the circuit and render these properties as an intensity of a pixel. Instead, a mesh generated over the entire circuit and the mesh elements are employed for a partial differential equation analysis.
- b) The pixels are employed to evaluate the design of the circuit, e.g., based on the appearance of a pixel map. Nowhere in Lorenz is such a concept disclosed or suggested.
- c) The finite element method disclosed by Lorenz does not disclose or suggest discretizing a design representation into pixel elements representative of a structure in the design where each pixel element represents a portion of the design.
- d) In addition, Lorenz fails to disclose or suggest determining at least one property of each pixel element representing the portion of the design where the at least one property is represented by an intensity of the pixel element.

Examiner respectfully disagrees for the following reasons:

As to a) Lorenz discloses a CAD method of automatic mesh generation for integrated circuit design (MEMS) including mesh generator, wherein mesh generator includes computer instructions describing how to create a **mesh for each component (finite element/pixel element)** of the integrated circuit (MEMS) design (paragraph [0010]), wherein the analysis of the MEMS design programmatically analyzes mesh density (intensity) of each individual meshes of corresponding component (pixel element/finite element) (claim 5 of Lorenz).

As to b) Lorenz discloses adjusting programmatically a **mesh density of each individual meshes** including analysis (evaluation) of the integrated circuit design (claims 4, 5 of Lorenz).

As to c) Lorenz discloses a method of the design integrated circuit (MEMS) by generating a mesh that represents a schematic MEMS design, wherein generating the mesh representing a schematic MEMS design includes generating a **plurality of individual meshes for the plurality of components (pixel elements)** of the schematic MEMS design (claim 4 of Lorenz).

As to d) Lorenz discloses a method of the design integrated circuit (MEMS) by generating a mesh that represents a schematic MEMS design, wherein generating the mesh representing a schematic MEMS design includes generating a plurality of individual meshes for the **plurality of components (pixel elements)** of the schematic MEMS design (claim 4 of Lorenz), wherein the analysis of the MEMS design programmatically analyzes **mesh density (intensity)** of each individual meshes of corresponding component (pixel element/finite element) (claim 5 of Lorenz).

Finally, Examiner maintains rejection of the claims 1-32 by Lorenz et al. and Corson et al. individually and as a combination since they read in claims 1-32.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

[Handwritten Signature]
STACY A. WHITMORE
PRIMARY EXAMINER

Examiner Helen Rossoshek